Invited Talk at CCD'79 @ Edinburgh, Scotland UK

ADVANCES in CCD IMAGERS

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ABSTRACT

This paper provides a review of progress made in Sony on the technology and performance of CCD imagers for color video cameras. There are two basic approaches to realize a CCD image sensor, namely interline transfer organization and frame transfer organization. Sony has undertaken the design and fabrication of both types of the CCD imagers, and the development effort resulted in four different versions of CCD imagers. They are (1) a 242Hx 494V interline transfer CCD imager with high density structure,(2) zigzag-transfer CCD with checker-pattern sensing sites,(3) a 242Hx490v CCD imager with SiO2 exposed photo-sensing arrays in frame transfer organization and (4) a 380^x 488^ F.T. CCD imager with narrow channel transfer gates. In this paper, the designs and operations of these CCD imagers and their camera systems are described in detail.

I. INTRODUCTION

On March 9, 1978, Sony Corporation announced the development of an epoch making small size color video camera, utilizing newly developed large scale charge-coupled device technology. The camera was developed in its Research Center and the Semiconductor Development Division. The charge-coupled device (CCD) contains about 111,192 elements on a single chip, and serves as the image sensor for the camera in place of the traditional pickup tube. Among the first companies to predict the importance and future applications of CCD technology, Sony has concentrated its efforts on combining company's technological leads in integrated semiconductors, crystallization and image sensing, and was able to produce an actual product using the newly developed CCD technology. The CCD camera is capable of a picture quality close to ideal, and provides reliability and stability greater than current pickup tube cameras. With camera size and weight reduced to that of an 8mm camera, and picture quality that of current top range video cameras, an entirely new video camera can be brought to life. The CCD chip (.1) measures 10. 3mm by 9.1mm, with each element 36um by 13pm, arranged in a matrix of 226 horizontal elements by 492 vertical elements, for a total of 111,192 picture elements. The CCD camera will contain 3 chips, and by utilizing Sony's original Spatial Offsetting Technique, which allows a doubling of horizontal resolution, provides for greatly increased picture resolution. By developing such structural facets as interline transfer organization, buried channels, and Sn02 transparent electrodes, improvements in picture quality, resolution, sensitivity and signal to noise ratio were made possible. As a result, even with a 2/3-inch optical system, extremely high standards such as greater than 280 line horizontal resolution and 700 lux minimum scene illumination (at F2) were achieved.(2)

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The basic technological advancement to achieve the CCD camera has been carried out in the early development of another color camera which utilizes zigzag-transfer CCD imagers (3) with checker-pattern sensing site, with 142 horizontal pixels(p =62j*m) and 492 vertical pixels (p„-13/um) . The standard 2/3-inch format of the optical system leads to a CCD chip size of 10 mm x 8.2 mm. Horizontally, 270 TV lines per picture height can be resolved, and 350 TV line/ph vertically.(4) The scene illumination was 8,000 lux through poly-Si photo sensing electrodes, to obtain the signal-to-noise ratio of about 40 dB, for color temperature of 3,200°K, an aperture of F2, and 90% reflectance. The scene illumination is expected to be reduced to 2,000 lux from the data of the spectral response of a black and white camera using the zigzag transfer CCD with Sn02 transparent photo sensing electrodes. Anti-blooming control is effective up to 100 times over saturation at the wavelength of 448 nm. As a matter of fact, before undertaking the developments of the above mentioned two image sensors, Sony has worked with a simpler structure of CCD imager, namely a frame transfer CCD with Si02 exposed photo sensor arrays. (5) In the imaging area, an SiC2 exposed photo sensor of 13 um x 6/4ip is located in a CCD unit cell of 36juni x 13/^m. Photon-generated charges at the photo sensor are collected under the storage gate by diffusion and drift due to the fringing field of the storage gate, and are transferred in the vertical shift register. The quantum efficiency of 55% has been obtained at 450nm wavelength in the spectral response of the photo sensors. The fat "1" storing part is introduced to improve the transfer efficiency of the vertical shift registers. In the constructed color camera using three CCD chips, offsetting the RED and BLUE CCD chips spatially by 1/2 pixel with respect to the GREEN in the horizontal direction, the horizontal image resolution of 280 TV lines/ph has been obtained.(6)

The development of F.T. CCD imager was further enhanced by the realization of the 380H x 488V CCD imager with narrow channel transfer gates.(7) It consists of 380 x 244 bit imaging area, 380 x 244 bit storage area, and 380 bit horizontal readout shift register. In the imaging area, an Si02 exposed photo-sensor window of 21/tm x 6^m is located in the CCD unit cell of 24/im x 14^m. The chip size of the device is 10.1 mm x 14.6 mm in which the imaging area is 8.8 mm x 6.6 mm determined by 2/3 inch picture format of the optical system. The transfer efficiency of the vertical and horizontal shift registers are more than 99.995% per transfer. And high image resolution of 280 TV lines/p.h. (Horizontal) and 350 TV lines/p.h. (Vertical) have been obtained. The dark current level is less than 3% of the maximum signal level at the room temperature of 20°C. The spectral response of the imager is also analyzed and reported. It is expected that this inherently Si02 exposed structure has high enough quantum efficiency at 450nm wavelength and functions as a color imager with high sensitivity and resolution.

The principles and methods of designing solid-state imagers are now well understood but the ultimate key to realize high resolution, high sensitivity and low-cost solid state imaging devices is the fabrication technology. And the processing success is measured by the yield. Imaging devices, like all other integrated circuit products, are expected to fall on a steep learning curve.

II. A 242H x 494V Interline Transfer CCD Imager with High Density Structure

The imager consists of 226 horizontal picture elements and 492 vertical picture elements in a 2/3 inch optical system. Sn02 electrodes are employed as photo sensors and give high sensitivity for blue light. The buried channel CCD imagers with two-phase clock operation have high transfer efficiency and low noise. The transfer efficiency observed is 99.996% per stage. The chip size of this device is 10.3 mm x 9.1 mm with a unit cell size of 36/un x 13/*m. The comparison of spectral sensitivity of the CCD imager with SnO electrodes

and that with conventional polysilicon electrodes can be seen in Figure 1. The CCD with polysilicon electrodes is known to have low sensitivity for blue light which limits the sensitivity of CCD color cameras. In contrast, the Sn02 electrodes used for our CCD imagers increase the sensitivity of the blue channel by five times compared with polysilicon elect).odes. Due to the excess charge generated under intense optical overloads, blooming spread are observed along the vertical direction in the picture. To prevent these blooming effects, overflow drains have been employed which absorb the excess charge overflow in the vertical registers of the CCD imager. The overflow drains, capable of containing 20 times optical overloads, are confirmed to have good anti-blooming functions. The overlapping of baseband signals and sideband signals, associated with spatially discrete sampling by the color filter, is observed in the output signal of some conventional single tube color cameras. This overlap is observed particularly, often to a remarkable extent, when color scenes are scanned. Generally speaking, however, the actual degradation of the picture quality is small due to the following considerations:

(a) Many objects and scenes are low in saturation. (b) Even in a picture with high color saturation, the disturbance is small because of the spurious signals appear mainly on the contours of the objects seen, that is, high frequency components have most effect on the edges or contours. The above considerations show that the bandwidth of the luminance signal can be effectively expanded by applying the coding technique of single tube cameras to the multi-chip CCD camera. The frequency response of a CCD is illustrated in Figure 2. It shows aliasing errors associated with spatially discrete sampling of a photo sensing imager. In order to eliminate these errors, an optical low pass filter is usually employed and limits the bandwidth to 1/2 f _ where f stands for the sampling frequency. But, when the GREEN chip is displaced by half the pitch of the horizontal separation of picture elements as shown in Figure 3, the phase of the sideband signals of the GREEN chip is delayed by 180° with respect to that of the RED and BLUE chips. At the same time, when the signal level of each CCD satisfies the following condition, 0.33R + 0.17B = 0.5G the spurious spectra of RED,BLUE and GREEN CCD chips are cancelled out as shown in Figure 4. Especially in the case of picking up of black-and white scenes, the effective bandwidth of the luminance signal reaches the maximum possible for the multi-chip CCD color camera, that is for our case twice the bandwidth of a single chip. This effect of the spatial offsetting technique has been confirmed in the constructed camera. The block diagram of the constructed camera is shown in Figure 5. The 2/3-inch optical system is employed, consisting of a zoom lens and a prism. CCD output signals are connected to sample-hold circuits and pass through auto white balance circuits and processors and are converted to NTSC signals in the encoder. The horizontal clock frequency is 4.77MHz. The clock is derived from the 14MHz (4fsc) clock generator. Each blemish of the CCD imager is replaced by the signal of the picture element just before the defective one. Addresses of the blemishes are stored in the PROM as relative addresses. Luminance signal and chrominance signal are separately processed. Due to the spatial offsetting technique, luminance signal Y is given by: Y = 0.33R + 0.5G + 0.17B Auto white balance circuits are controlled by digital memories. As control signals for the auto white balance circuits, (R-G) and (B-G) are used. These signals are also employed as color difference signals to the encoder. Figure 6 shows the overall normalized spectral response. The picture produced by this camera is shown in Figure 7.

III. Zigzag Transfer CO with Checker-Pattern Sensing Sites

The zigzag-transfer CCD's employing checker-pattern sensing sites have been developed to reali.ve the novel image sampling technique. The schematic layout of the structure is shown in Figure 8. Two vertical photo sensing columns share one vertical shift register and one overflow drain. Compared with the interline transfer CCD, the photo sensing areas are thus enlarged. Also the amount of handling charge of the vertical shift registers is increased. Transfer bits of the horizontal shift register are reduced and the driving frequency can be lowered. Because of the pattern tolerance about overflow drains, the anti-blooming control is easy to be built in, and the functions of automatic gain control and varying gamma correction can also be incorporated on a CCD chip.

In the conventional frame transfer and interline transfer CCD imagers, photo sensing sites are arranged in square sampling scheme as shown in Fig. 9(a). Many carriers of an output image are generated in the spectrum spaceas shown in Fig.9(b), where p is the sampling period, u,v, and w are the angular frequencies in the horizontal(x), vertical(y) and timing(t) directions of output images respectively. Interlacing of 1:2 removes the carriers marked with white dots from the plane p w/2ir-n (n: an integer) to the plane p w/2?r=(2n+1)/2. Carriers marked with black dots remain on the former plane.

In Fig.10(a), the same number of CCD pixels as the conventional scheme in Fig.9(a) are arranged in a checker-pattern, and sensing sites of the RED CCD, and the BLUE CCD are offset by p and p„. , respectively, with respect to those of the GREEN CCD. Carrier positions of sampled images in CCD's are obtained by Fourier transform as shown in Fig.10(b) . The carriers on the line p V/2TT=1/2 disappear from this plane as described above.

The condition for eliminating carriers on the lines p^u/27r=n (n: an integer) by spatial offsetting of sampling sites among three CCD's is A + A exp(-j27rnp /p) + A, exp (-j 2vrnp ,/p) - 0. g r L J Lxr/Lx b ^ J xb' x Balancing conditions for n=l,2,4,5,7,... are selected for black and white images, where high resolution is necessary. Only carriers marked with black dots thus remain in Fig.10(b). The horizontal rows of pixels are complemented interstitially with upper rows by means of a one line delay element. This signal processing is limited to the frequency region higher than u of about 1 MHz, because the spectra near the point (p U/2TT,P V/2TT) = (0,1/4) contribute greatly to the vertical resolution. $he aliasing errors are faded out near the hatched region along the line p v/2?r =1/4 shown in Fig.10(b).

When the rest of aliasing Errors on the line 9^U/2TT= 1 without vertical correlation are detected, a band eliminate filter depresses aliasing errors near the hatched region along the line p V/2TT=1 as schematically shown in Fig.10(b).

Due to the nature of object images and human eyes, the spectra along the u-axis and v-axis are most important for producing a high resolution image. In addition, the sprctra of the region 0^p U/2JT^1.5 or 2 on u-axis and of the region 0^p v/2;rg0.5 on v-axis are obtained. Therefore, compared with the conventional scheme in Fig.10, horizontal resolution is improved^ by a factor of two or more employing the same number of pixels while vertical resolution remains the same. Aperture effects of sampling functions should be selected suitably for this band limited signal, both spatially and electrically. The image obtained
with this color camera is shown in Figure 11.

IV. A 242H x 490V CCD Imager with SiO exposed photo-sensing arrays

The device has been organized for a frame transfer CCD operated with two phase clocks and fabricated on a P-type (100) oriented, 2-3 ohm-cm silicon substrate in surface channel with overlapping polysilicon gate structure. Well-known silicon gate MOS technologies are used to fabricate the device. The gate oxide thickness and the channel length are 120nm and 9m for the storage gate, and 360nm and 4,/£m for the transfer gate, respectively. Phosphorus doped polysilicon with the sheet resistivity of 50-70ohin/a and the thickness of 500nm is used for the gate electrode material. To eliminate oxidation-induced stacking faults and other generation-recombination centers, high density (more than lxl020/cm3) phosphorus diffusion at 1,100°C and HC£ oxidation were employed. Aluminum metallization for the photo shielding, surrounding the photo sensor, is used to improve the image quality by an aperture effect. The spectral response of the Si02 exposed photo sensors and the photo sensors of polysllicon-Si02 are shown in Fig.12. A solid state color camera using three CCD chips has been constructed. A 2/3-inch lens and a prismatic assembly of dichroic beam splitters are employed in this system. The resolution of the CCD camera is limited by the aliasing errors associated with spatially discrete sampling of the image on a photo sensing area. Offsetting the Red and Blue CCD chips spatially by 1/2 pixel with respect to the Green in the horizontal direction, the aliasing errors can be suppressed by cancelling out the spurious spectra of the Red, Blue and Green CCD's in the spatial frequency response. As a result, the horizontal image resolution of 280 TV lines/p.h. has been obtained with relatively small 242 bit horizontal pixels. Figure 13 shows a photograph of the TV picture of an image.

V. A 38011 x 488v CCD Imager with Narrow Channel Transfer Gates

When the channel width of an FET becomes of the same order of magnitude as the depth of the gate depletion region, an increase of threshold voltage is observed. This narrow channel effect has been applied successfully in creating an asymmetrical potential well under an electrode for two phase CCD operations. Figure 14 shows cross sectional views of the electrode for two phase CCD structure. For the structure fabricated, each electrode of the horizontal readout register has one large storage region of 70.um width and seven narrow-channel transfer regions of 3/<m width. The channel lengths of the storage and transfer parts of the electrode are 7am and 5jum respectively. Each electrode of the vertical shift register has one large storage region of 18.um width and one narrow-channel transfer region of 3,um width. The channel lengths of the storage and transfer parts of the electrode are 8tan and 6/im respectively. The width of the channel stop between vertical registers is 6/cn. Fig.15-17 show the unit cell of the imaging area, the horizontal readout register, and TV pictures of scenes.

The spectral response of the imager is analyzed and reported in Fig.18, and the operating conditions of the CCD imager are listed in table I. As seen in Fig.19 of the actual measured channel potentials plotted against the gate voltage for the buried channel version, no clock overlap is necessary both for the vertical and horizontal shift registers. This simplifies drastically the construction of a timing system for the imager.

VI. Conclusion Four different versions of CCD imagers developed in Sony are reviewed. When the goal is set to a chip size of 1cm by 1cm or more, the present technological progress of large integrated circuits seems very slow. Nevertheless ,the improvement is solid and steady, and so is our effort.

Acknowledgement

The author is indebted to colleagues of Semiconductor Division for their fruitful collaboration and discussions. He is also grateful to H. Yoshida, H. Yagi, Y. Kawana, K. Nakamura, M. Kikuchi, and K. Iwama for their encouragement and variable suggestions throughout the course of this project. Coworkers of this paper are listed in the reference with sincere gratitude and respect.

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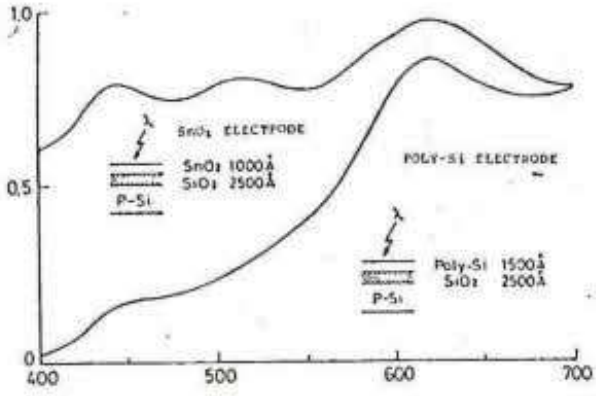

Fig. 1. SPECTRAL RESPONSE OF CCD

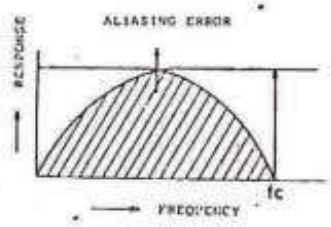

Fig. 2. FREQUENCY RESPONSE OF A CCD

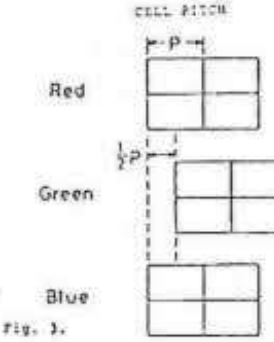

Fig. 3. RELATIVE POSITION OF THREE CCD'S FOR SPATIAL OFFSETTING TECHNIQUE

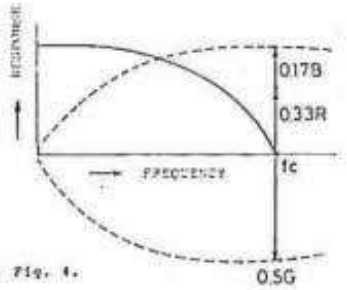

Fig. 4. FREQUENCY RESPONSE OF LUMINANCE SIGNAL IN SPATIAL OFFSETTING TECHNIQUE

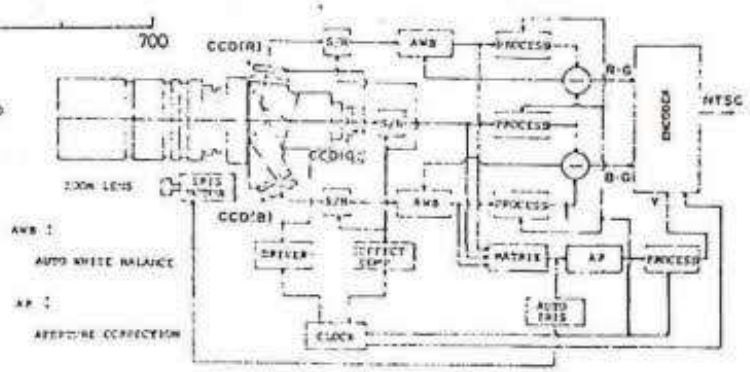

Fig. 5. BLOCK DIAGRAM OF THE SYSTEM

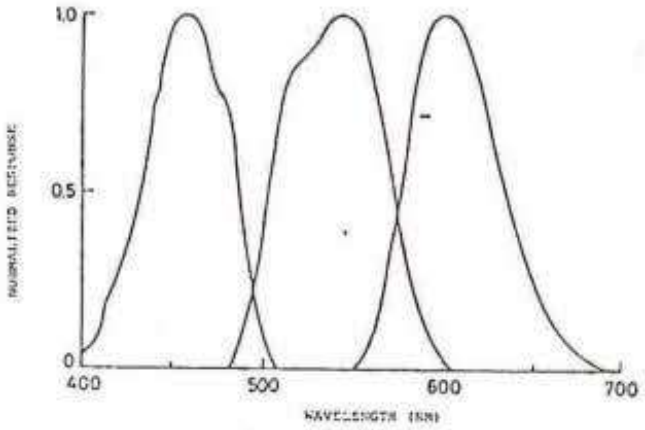

Fig. 6. OVERALL SPECTRAL RESPONSE

Fig. 7. Image produced by the color camera

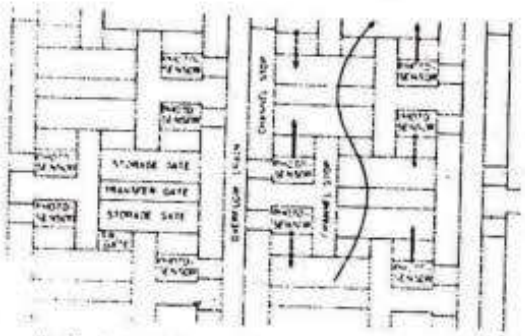

Fig. 8 Schematic layout of zigzag transfer CCD structure.

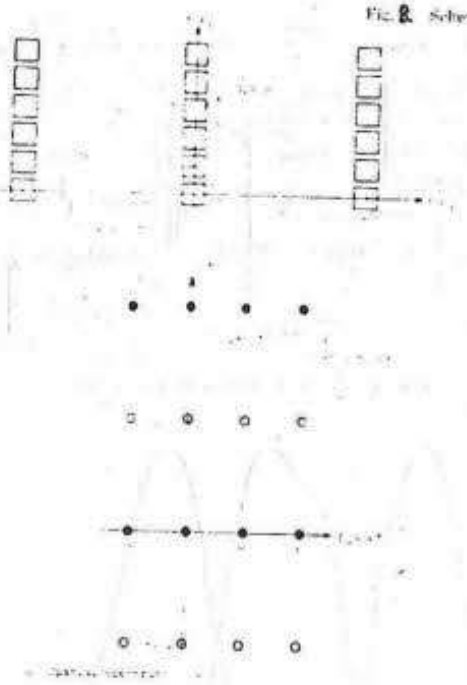

Fig. 9 Sensing sites for square sampling and its spatial spectrum

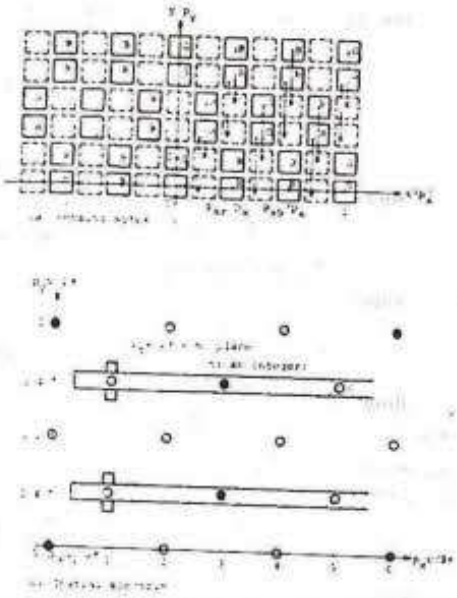

Fig. 10 Sensing sites for checker-pattern sampling and its spatial spectrum

Fig. 11 Image produced by the color camera with three 142 × 492 element zigzag transfer CCD imagers employing the novel image processing technique.

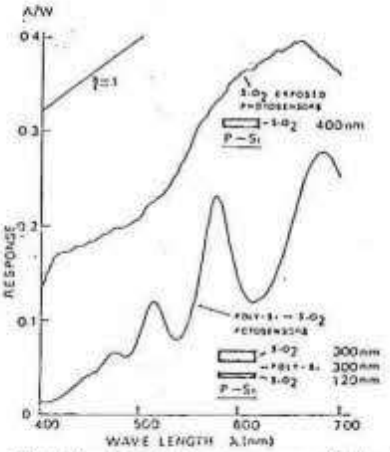

Fig. 12a Spectral response of the photosensors

Fig. 13 A TV picture of an image

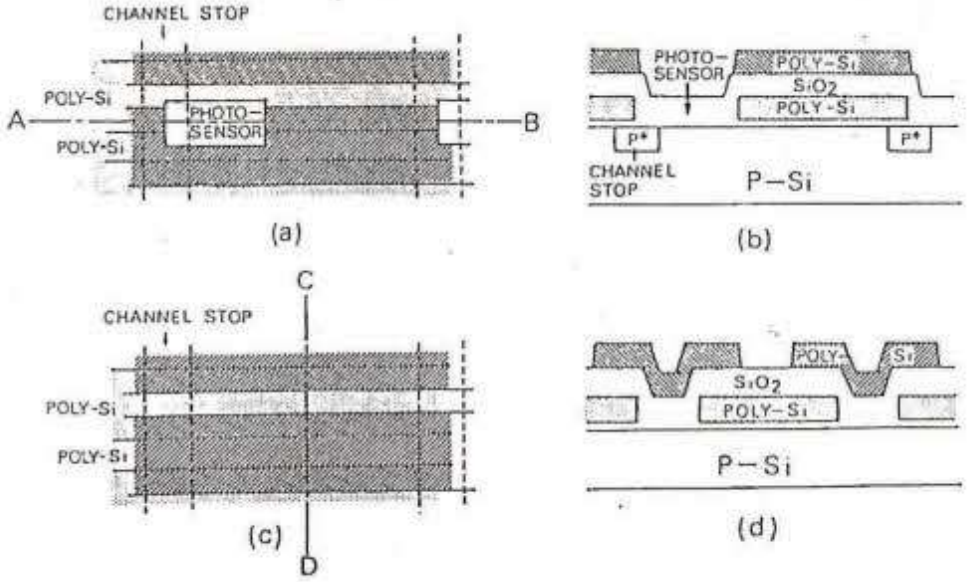

Fig. 12b Structures of the unit cells of the imaging and storage area
(a) A unit cell of the imaging area
(b) A cross-sectional view of (a) along a line A-B
(c) A unit cell of the storage area
(d) A cross-sectional view of (c) along a line C-D

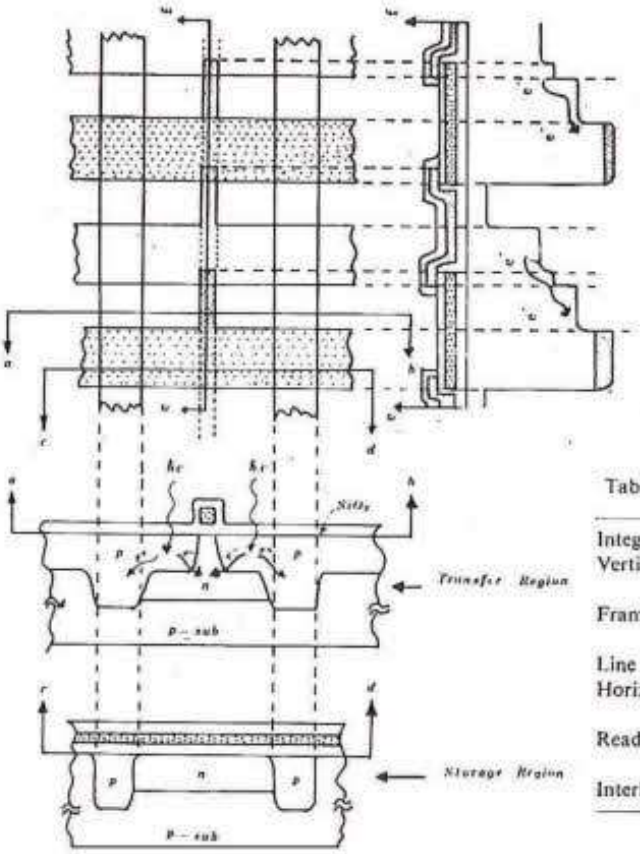

Table I. Operating conditions of the CCD imager.

Integration time	16 msec
Vertical clock voltage	from −2 volt to −12 volt
Frame shift frequency	14.31818 MHz/32 =447.4 KHz
Line shift frequency	15.7 KHz
Horizontal clock voltage	from 3 volt to −12 volt
Readout frequency	14.31818 MHz/2 =7.15909 MHz
Interlace	2:1

Fig. 14 Top and cross sectional views of the electrode for two phase CCD structure.

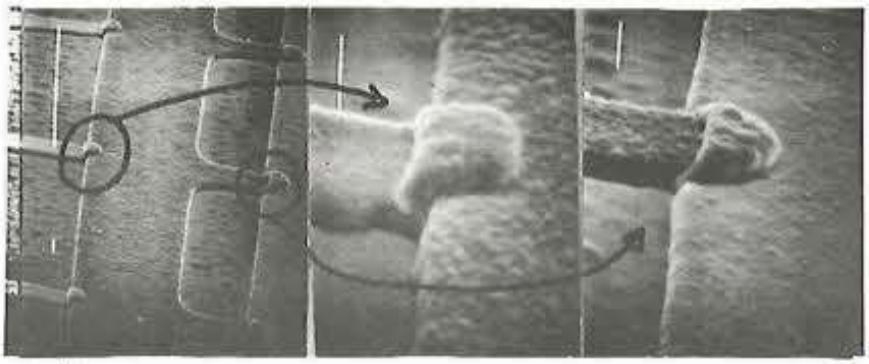

Fig. 15 SiO_2 exposed photo-sensor window of 21 $\mu m \times 6$ μm located in the unit cell of 24 $\mu m \times$ 14 μm. The width of the narrow channel is 3 μm throughout the device. The electrode overlap is 2 μm.

Fig.16. The horizontal readout register with 14 μm-pitch-per bit electrode structure.

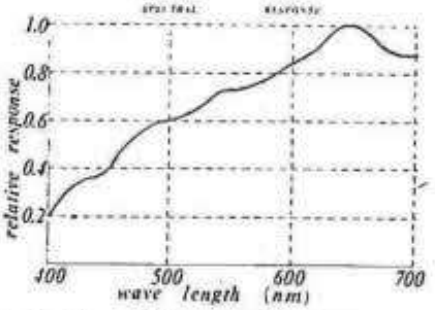

Fig. 18. Spectral Response of the photosensors.

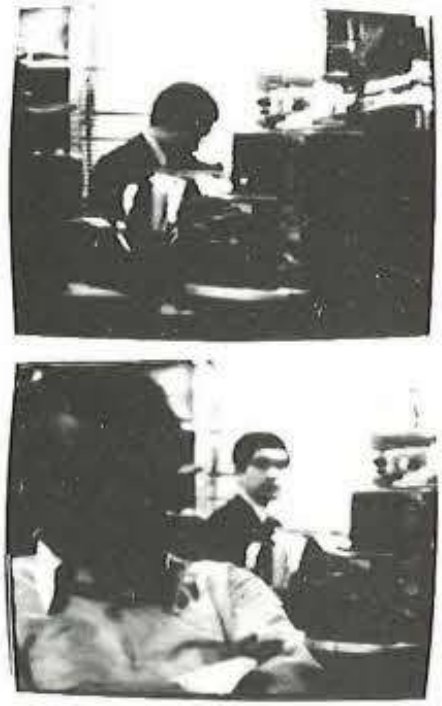

Fig. 17 TV pictures of scenes against light. Anti-blooming effects seem working. The maximum light intensity through the lab-window corresponds to about ten times of the maximum handling charge of the imager.

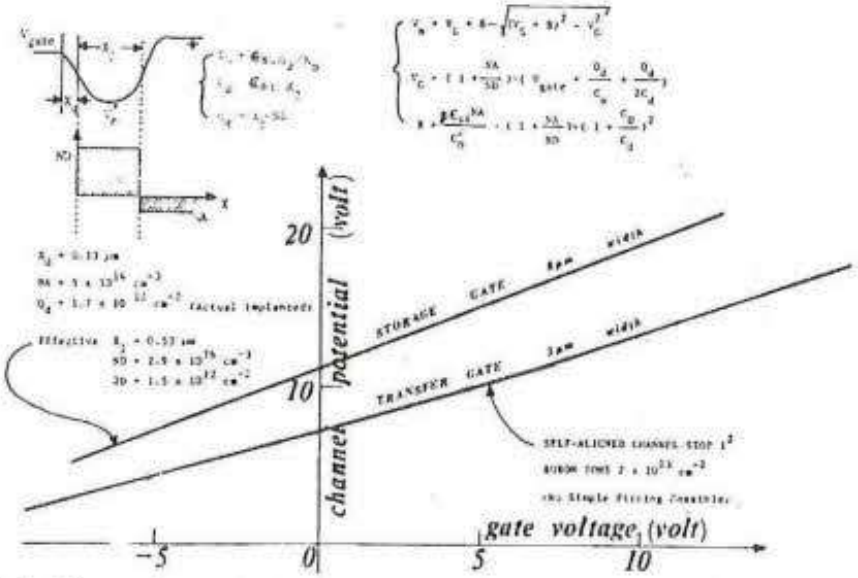

Fig.19. The actual measured channel potentials plotted against the gate voltage for the buried channel version. The curve fitting with the simple relations by depletion approximation gives the effective values of X_j, ND and QD as seen in the figure.